Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A data processor comprising one or more functional units, one or more register files, a data memory, and a snapshot buffer which during ~~the~~ handling of an interrupt condition accommodates to save state ~~informations~~information of various processor state elements in respective snapshot buffer elements,

said data processor ~~being characterized by~~ comprising controller means ~~that are~~ arranged ~~for upon a subsequent interrupt condition that occurs during the handling of an actual interrupt condition saving~~to save the contents of said snapshot buffer elements in a data memory facility having a multibit access port facility upon a subsequent interrupt condition that occurs during the handling of an actual interrupt condition without requiring additional instruction bits for addressing the snapshot buffer elements or the data memory facility.

2. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, wherein said controller means are arranged ~~for upon completing the handling of an actual interrupt condition retrieving~~ to retrieve the ~~earlier~~ saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements upon completing the handling of the actual interrupt condition.

3. (Currently amended) ~~A~~ The data processor as claimed in Claim 2, wherein said controller means are arranged ~~for upon said retrieving likewise restoring~~to restore ~~earlier~~ the retrieved saved state ~~informations~~information of various processor state elements allowing said data processor to proceed with handling one of an earlier uncompleted interrupt~~, or, as the case may be to proceed with~~ or continuing a main thread of the processing.

4. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, wherein said state ~~informations~~information comprise latency data of current operations.

5. (Currently amended) AThe data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring ~~their contents~~ to said data memory facility.

6. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring ~~their saved contents~~ from said data memory facility.

7. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, wherein said data memory facility is operated as a stack.

8. (Currently amended) ~~A~~ The data processor as claimed in Claim 7, wherein said stack has a stack pointer that allows multiple stack positions per snapshot.

9. (Currently amended) ~~A~~ The data processor as claimed in claim 7, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility, and wherein write and read operations in said stack are executed at mutually exclusive instants in time under control of a stack pointer.

10. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, wherein said snapshot buffer is at least substantially constructed from shadow flipflops for storing its snapshot information.

11. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, wherein said snapshot buffer is operated at low power through one or more of clocking shadow flipflops only during actual taking of a snapshot, ~~which may imply activating the snapshot buffer during only one clock cycle,~~ clocking only ~~the~~ shadow flipflops pointed to by ~~the~~ a stack pointer as ~~the~~ a top-of-stack-plus-one during a stack push operation, and clocking the stack pointer itself only during stack pointer updates that are caused by ~~the~~ popping

and pushing~~, respectively,~~ of ~~the~~ a snapshot buffer stack.

12. (Currently amended) ~~A~~ The data processor as claimed in Claim 1, having a plurality of parallel issue slots ~~(32-38)~~ of which only a single issue slot is used for implementing ~~such~~ handling of nested interrupts.

13. (Currently amended) A data processing facility comprising ~~an embedded~~the data processor as claimed in Claim 1.

14. (Canceled)

15. (New) The data processing facility as claimed in claim 1, wherein the controller means is arranged to save the various processor state elements to the respective snapshot buffer elements in a single clock cycle.

16. (New) The data processing facility as claimed in claim 1, wherein the controller means is arranged to restore the various processor state elements from the respective snapshot buffer elements in a single clock cycle.